IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

THE TRUSTEES OF PURDUE UNIVERSITY,

Plaintiff,

vs.

STMICROELECTRONICS N.V., ET AL.,

Defendant.

NO. 6:21–CV–727–ADA

JURY TRIAL DEMANDED

ST MICROELECTRONICS, INC.'S[1] REPLY CLAIM CONSTRUCTION BRIEF

[1] Purdue also names as defendants STMicroelectronics N.V. ("STNV") and STMicroelectronics International N.V. ("ST Int'l"). STNV is not subject to the Court's jurisdiction, as detailed in its Motion to Dismiss [ECF 38], and ST Int'l has not yet been served in this case and therefore is not properly before the Court or subject to the Court's jurisdiction.

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EXHIBIT LIST

Responding Declaration of Vivek Subramanian, Ph.D. ("Subramanian Rebuttal Decl."), with attached Exhibit 1

Ex. A: U.S. Provisional Application No. 61/047,274

Ex. B: Excerpts from B. Jayant Baliga entitled Power Semiconductor Devices ("*Baliga*")

Ex. C: Original claims, U.S. Patent Application Ser. No. 12/429,176

Ex. D: Sept. 22, 2010 Office Action from Prosecution History of U.S. Patent Application Ser. No. 12/429,176

Ex. E: May 23, 2011 Response to Office Action from Prosecution History of U.S. Patent Application Ser. No. 12/429,176

Ex. F: Excerpts from Petition for IPR of '633 Patent (IPR2022-00252)

Ex. G: Excerpts from Petition for IPR of '112 Patent (IPR2022-00309)

A. The second, thicker oxide layers in claims 1 and 6 of the '112 Patent must be an oxidation layer of the type that is formed, created, or grown by reacting the gate.

1. ST's construction identifies an essential structural characteristic of the oxide layer.

Purdue wrongly accuses ST of improperly introducing a method step in an apparatus claim. ST is not importing a process step. To the contrary, ST's construction describes *structure* ("an oxidation layer") of a certain *type* ("formed, created, or grown by reacting the gate"). This language describes an essential characteristic of the oxidation layer based on its formation (like "dry-aged" steak, "cold-brew" coffee, or "forged" steel). There is nothing improper in describing the claimed apparatus structure this way, and the patent itself does that repeatedly, including it its ***title***: "SiC Power DMOSFET With ***Self-Aligned*** Source Contact." Just like "self-aligned" is a structural characteristic of the source contact region based on its formation, "formed, created, or grown by reacting the gate," is a structural characteristic of the oxidation layer. Neither description improperly introduces a process step.

ST's construction precisely mirrors the scope of the invention defined by the patent. Purdue argues that ST "attempts to restrict the claims to a single method of making one particular embodiment" and "nothing in the specification or claim language restricts how the products are made." (Resp. at 6–7.) But ST's construction is *dictated* by express restrictive language in the specification. While the specification says, in view of the many manufacturing steps, the product's fabrication "can be accomplished in a variety ways" (e.g., with different materials, times, temperatures, and conditions), with respect to the oxide layer at issue, the specification **disavows** any alternatives in which the layer is the type not formed, created, or grown by reacting the gate: "Alternative embodiments [to the overall manufacturing process] are contemplated . . . ***so long as the gate and substrate source (or other ohmic contact materials) react to form, create or grow an insulation layer (such as SiO_2)*** sufficiently faster, larger and/or with more insulating capacity at the gate surface than at the substrate surface." '112 Patent at 7:20–33 (emphasis

added). Purdue fails to address this explicit disavowal, and its construction improperly reclaims that which has been disclaimed. And Purdue likewise ignores the patent's repeated identification of "the present invention" as a DMOSFET with "self-aligned source contacts," which are enabled by *growing* the oxide layer around the gate (as opposed to the disfavored approach of using a deposited oxide layer, then creating an opening using a mask).[2] The provisional application for the '112 patent, which is incorporated by reference, likewise describes the necessity of using a grown oxide. *See* '112 Patent at 1:7–9; **Ex. A**.

Additionally, the specification incorporates by reference a textbook by B. Jayant Baliga entitled Power Semiconductor Devices (hereinafter, "*Baliga*") that further demonstrates ST's construction is correct. '112 Patent at 1:45–49.[3] *Baliga* shows and describes a conventional process in a power MOSFET for covering the polysilicon gates with a ***deposited*** oxide and then "patterning" the oxide using a mask before depositing the source electrode as a layer.[4] The book explains, "[t]he oxide layer is now patterned to form the contact windows as illustrated in Fig. 7.53(d). This [step] is another critical photolithographic step in the DMOS process because misalignment can either cause poor contact to the p-base region or lead to an overlap of the contact with the polysilicon at the cell edges. This overlap will produce a short between the source and the gate." *Baliga* at 411–12; Fig. 7.53. This problem, specific to deposited oxides, is the precise problem the '112 Patent attempts to solve by instead using a grown oxide technique. '112 Patent at 2:18–20. This description in *Baliga*, and the alternative in the patent of growing an oxide (5:61–6:56), are both intrinsic to the patent and provide a clear contrast between (a) using a deposited oxide, which requires patterning (using a mask), with the associated risk of

[2] *See* ST's Opening Brief (ECF No. 66) at 6–11.
[3] Because the book is incorporated by reference, it is intrinsic evidence to the patent.
[4] **Ex. B**: Excerpts from *Baliga* at 411–12 and Fig. 7.53.

misalignment, and (b) using a grown oxide, which avoids the misalignment problem and is the purported invention of the patent. *See* Subramanian Rebuttal Decl. ¶¶ 9–13.

Purdue agrees an invention is properly limited when the patentee manifests a clear intention to restrict the claim scope to a particular embodiment. (Resp. at 7 (citing *Info-Hold, Inc. v. Applied Media Techs. Corp.*, 783 F.3d 1262, 1267 (Fed. Cir. 2015).) Here, the patent ***does*** in fact manifest a clear intention to restrict the invention to an oxidation layer formed, created, or grown by reacting the gate, which permits a contact self-aligned to the gate without any mask. Purdue fails to cite any cases to support its argument that importing a process step is improper even when the patentee makes the process step essential to the claimed invention.

2. Even if characterized as implicating a process, the patentee has made clear that growing the oxidation layer is an essential part of the claimed invention.

The Federal Circuit has repeatedly held a process disclosed in a specification "can be treated as part of a product claim if the patentee has made clear that the process steps are an essential part of the claimed invention." *Andersen Corp. v. Fiber Composites, LLC*, 474 F.3d 1361, 1375 (Fed. Cir. 2007). For example, in *Southwall Techs., Inc. v. Cardinal IG Co.*, 54 F.3d 1570 (Fed. Cir. 1995), the court held that a claim to a dielectric layer was "limited to a dielectric layer prepared by a one-step process" because the patentee excluded those formed by a two-step process.[5]

As explained in ST's opening brief, the specification unambiguously states that the invention is to be broadly construed ***so long as*** the insulating oxidation layer around the gate is limited to one that is ***formed, created, or grown by reacting the gate*** because this is how the patent allegedly achieves the purported invention ("self-aligned source contacts").[6] The alternative—a deposited oxide layer—only presents the very problem the patent attempts to

[5] *Anderson*, 474 F.3d at 1375 (discussing the *Southwall Technologies* case).
[6] *See* ST's Opening Brief (ECF No. 66) at 9–10.

solve.[7] Accordingly, just like in *Anderson* where the "***dielectric layer***" was limited to one "***prepared by a one-step process***," here the "***oxide layer***" must be limited to one "***formed, created, or grown by reacting the gate***" because it is essential to the claimed invention.

3. The Applicant's election of the product claims over the method claim during prosecution does not support Purdue's argument.

The prosecution history does not support Purdue's construction (and in fact supports ST's). By way of background, the original application included a set of product claims ("Group I") and a method claim ("Group II"). The Group II method included the steps of (1) "oxidizing" the polysilicon gate and the SiC substrate "to form a second oxide layer having substantially greater thickness over said gate than over the silicon carbide," and then (2) "etching said first and second oxide lawyers without a photomask."[8]

Purdue's argues that the PTO required the Applicant to choose between the Group I product claims and the Group II method claim because the inventions are distinct. Purdue suggests (without actually stating) the inventions were distinct because the oxide layer in the products could be made by a process other than reacting the gate (i.e., by depositing oxide). But this is not what the Applicant told the Examiner or what the Examiner understood. Conversely, the Examiner explained that the Group I products could be made in different ways than the Group II method, not because they could be formed by depositing the oxide layer, but because *there are different ways to etch without a photomask* (relating to method step (2), above).[9] Neither the Examiner nor the Applicant claimed the oxide layer in the Group I products could be formed by any method other than reacting the gate. This aspect of the product fabrication did not prompt the restriction requirement. Purdue's reliance on the prosecution history is misplaced.

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[7] *See, e.g.*, '112 Patent at 2:19–21, 3:57–59, 6:63–7:2.
[8] **Ex. C**: Original claims (annotating the steps at issue in yellow).
[9] **Ex. D**: Sept. 22, 2010 Office Action at 2.

In fact, the prosecution history *supports* ST's construction that the oxide layer in the product claims must be formed, created, or grown by reacting the gate. On October 22, 2010, the Applicant elected to prosecute the product claims and canceled the method claim. Even *after* this election, the Applicant confirmed to the PTO how the *growth* of the oxidation layer in the *product* claims is an essential characteristic of the claimed invention (in order to distinguish the prior art):

> **[A]pplicant's invention provides for** a SiC substrate and polysilicon gates because **growth of the oxidation layer** on the polysilicon gates occurs considerably faster than on the SiC substrate, which creates a much thinner combined oxide layer between adjacent gates (as shown in Fig. 7 of the application) than is simultaneously formed on the tops and sides of such gates. Thus, after a short oxide etch is applied, long enough to completely remove the thin, combined oxide layer over the substrate surface (and between the gates), there is still left a very thick insulating oxide layer on the tops and sides of gates. **This is more than an obvious design choice and is nowhere disclosed, taught or suggested by Miura**.[10]

ST's construction should be adopted, because it properly reflects the invention as a whole, including specific disavowals that the patentee made throughout the intrinsic record to describe the claimed invention and distinguish it from the prior art in order to obtain its allowance.

B. The preamble of claim 9 of the '633 Patent is limiting.

1. Purdue resorting to the specification to supply meaning and structure missing from the claim body confirms that the preamble is limiting.

Purdue concedes that a preamble is limiting when it recites essential structure of the invention. (Resp. at 8.) With respect to claim 9, Purdue does not dispute that the claim body is missing essential MOSFET elements, including a gate, gate insulator, and drain. Without specifying these elements, the claim could be read on other types of transistors. (Subramanian Opening Decl. ¶¶ 34–35.) Nonetheless, Purdue and its expert argue that a POSITA would know that claim 9 refers to a double-implanted MOSFET in silicon carbide without help from the preamble (even though the preamble recites a "double-implanted metal-oxide semiconductor

[10] **Ex. E**: May 23, 2011 Response to Office Action at 12.

field-effect transistor"). According to Purdue and Dr. Bhat, a POSITA would simply look to the specification and drawings (instead of the preamble) to figure this out. (Resp. at 8–9; Bhat Decl. ¶¶ 29–30.)[11] But Purdue's argument ***confirms*** ST's point: the claim body recites an incomplete structure, and the preamble is needed to fill in the gaps. By arguing that the *specification*—rather than the claim elements—would alert a POSITA to the fact that claim 9 is a double-implanted MOSFET, Purdue has admitted that the claim body itself is incomplete.

C. "Less than about three micrometers" in claim 9 of the '633 Patent is indefinite.

1. Dr. Bhat's unsupported opinions fail to show that a POSITA could determine the upper boundary with reasonable certainty.

As explained in ST's opening brief, how close the JFET width must be to 3 micrometers in order to still be considered "about 3" depends on the criticality of the measurement to the particular application. *See* ST's Opening Brief (ECF No. 66) at 16–17 (comparing the criticality of a "vertical pipe" measurement for a floating dock versus a launch rail for a space rocket). Purdue's only support for the upper limit of the range is a conclusory statement by its expert, Dr. Bhat, that a POSITA would interpret "about" as implying 3.0 JFET width with a 10% variation (so "about 3" means 3.3). (Resp. at 12; Bhat Decl. ¶ 31.) Purdue's argument is problematic for several reasons. First, Dr. Bhat does not support his 10% variation with any evidence from the specification, prosecution history, or even contemporaneous literature. Because Dr. Bhat's opinions are conclusory and unsupported, they should be disregarded.[12]

[11] The inconsistency of Purdue's argument is striking. For the '633 Patent, Purdue argues a POSITA would freely import a limitation from the preferred embodiment to conclude claim 9 is directed to a DMOSFET in order to negate the need for a preamble. In contrast, for the '112 Patent, Purdue argues it is improper to import from the specification a limitation (i.e., an oxidation layer that is grown as opposed to deposited) that the patent teaches is ***essential*** to "the invention" and where other embodiments are disclaimed. Purdue cannot have it both ways.

[12] *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1318 (Fed. Cir. 2005) ("[C]onclusory, unsupported assertions by experts as to the definition of a claim term are not useful to a court."); *Saso Golf, Inc. v. Nike, Inc.*, 843 F. App'x 291, 295–96 (Fed. Cir. 2021) (holding that the district court's underlying factual finding that a POSITA would not know the precise bounds of the

Second, nothing in the '633 Patent suggests that "about" is intended to address manufacturing accuracy as Dr. Bhat contends. The issue here is not analogous to going to the deli, asking for "about a pound of turkey," and realizing the clerk cannot be 100% accurate. To the contrary, the JFET parameter here is intended to have an effect on the performance of the device, but because the patent does not describe any performance goal (like "going to the moon in a rocket ship" in the vertical-pipe analogy), there is no indication how much the parameter can vary above the 3-micrometer value and still perform as intended.

Dr. Bhat suggests a POSITA would know a 3.0-micrometer JFET width is optimal for silicon carbide and would recognize capturing values close to the optimal width is the purpose of the JFET-width limitation. (Bhat Decl. ¶¶ 32–36.) But Dr. Bhat's reasoning is flawed. First, the claim itself contradicts his argument because it covers a range from 0 to "about 3," thus covering a wide range of non-optimal values less than 3 for no apparent reason. Second, the literature Dr. Bhat cites contradicts his opinion. For example, while *Ryu* concludes 3 micrometers is optimal for a particular application with a particular combination of voltages, thicknesses, and concentrations, claim 9 does not specify any of those design characteristics. Moreover, *Ryu* explains that when taking manufacturing variations into account a different JFET width of 5 micrometers (a 66.7% increase over 3 micrometers) may actually be *more* optimal. This contradicts Dr. Bhat's conclusions that a POSITA would understand "about 3 micrometers" to mean a maximum upper limit of 3.3 micrometers (3.0 + 10%). (Subramanian Rebuttal Decl. ¶¶ 15, 18.)

2. Purdue has not shown that a POSITA could determine the lower boundary—something greater than 0 but less than 1 micrometer—with reasonable certainty.

Purdue does not dispute that "less than about 3 micrometers" literally includes a zero JFET

disputed term was supported by the accused infringer's technical expert testimony, whereas the patentee's expert only offered conclusory testimony to the contrary).

width, but argues a POSITA would understand the JFET width could not actually extend down to zero. (Resp. at 13.) Regardless, Purdue does not point to anything in the intrinsic record or literature that would allow a POSITA to determine the lower boundary of the claimed range—something greater than 0 but less than 1 micrometer. Does the claim cover JFET widths of 0.001 or 0.0001 micrometers? If not, how can one determine the lower limit as of 2005? In addition, the same evidence Purdue cites for the proposition that "less than about 3 micrometers" would be understood by a POSITA to reflect an optimal JFET width shows that a JFET width less than 1 micrometer has a dramatic increase in resistance ($R_{on,sp}$), which would have a severely *negative* effect on performance. (*See* Bhat Decl. ¶ 35; Subramanian Rebuttal Decl. ¶20.)

Dr. Bhat opines that "the lower bound for JFET width is limited by the manufacturing process technology" (Bhat Decl. ¶ 36), but fails to explain what that limit is and whether it is a moving target as technology evolves. Even if it were limited to the manufacturing process technology that existed in 2005, neither Dr. Bhat nor the patent explain what those technological limits were or how a POSITA would have actually applied them. There is simply no indication (whether from the patent, prosecution history, literature, or expert testimony) explaining that the patentee intended to limit the upper or lower boundary of this range based on "manufacturing process technology." Nor is there any disclosure about where to draw the line between 0 and 1 micrometer. Instead, Purdue proposes a moving target: the lower limit is as small as someone is able to make a device until someone else is able to make one even smaller.

D. ST's IPR petitions do not undermine its positions in district court.

Purdue alleges ST "reversed itself" after arguing in its IPR petitions that the PTAB "need not construe any terms of the challenged claims to resolve the underlying controversy." (Resp. at 1–2.) But ST's positions in the PTAB are uncontroversial and do not contradict its positions in this case. Claim construction is performed in an IPR **only** to the extent necessary to resolve the

IPR. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co*., 868 F.3d 1013, 1017 (Fed. Cir. 2017). Consistent with that principle, ST merely stated no constructions are required because the prior art invalidates regardless of the constructions: "[G]iven the close correlation between the asserted prior art and the challenged claims . . . any reasonable interpretation . . . reads on the prior art."[13] This is not an admission for purposes of claim construction in this case.[14]

Similarly, ST's decision not to argue indefiniteness in its IPR petition for the '633 Patent is not an admission that "less than about micrometers" is definite. ST could not assert indefiniteness in its petition because IPRs are statutorily limited to prior-art patentability challenges under §§ 102 and 103. 35 U.S.C. § 311(b); *Samsung Elecs. Am., Inc. v. Prisua Eng'g Corp.*, 948 F.3d 1342, 1350 (Fed. Cir. 2020) ("[W]e hold that the Board may not cancel claims for indefiniteness in an IPR proceeding."). Also, ST is merely pleading in the alternative in this Court and the PTAB. "[A]lternative pleading before a district court is common practice, especially where it concerns issues outside the scope of *inter partes* review." *Target Corp. v. Proxicom Wireless, LLC*, IPR2020-00904, Paper 11 at 12 (PTAB Nov. 10, 2020) (finding "unpersuasive Patent Owner's argument that Petitioner seeks 'a second bit[e] at the apple' by arguing to the Board claims are taught by the prior art, but arguing to the district court that the claims are indefinite" (alteration in original)). Finally, the precise bounds of the term were irrelevant for the IPR because ST presented prior art clearly covering any potential interpretation,[15] whereas the issue

[13] **Ex. F**: Excerpts from Petition for IPR of '633 Patent (IPR2022-00252) at 38–39; **Ex. G**: Excerpts from Petition for IPR of '112 Patent (IPR2022-00309) at 34.

[14] *See, e.g.*, *GoPro, Inc. v. C&A Mktg., Inc.*, No. 16-CV-03590-JST, 2017 WL 3131449, at *5 n.4 (N.D. Cal. July 24, 2017) ("The Court agrees with C&A that its arguments in its petition for [IPR] that the claims required no construction do not constitute an admission for purposes of the claim construction in the district court litigation. As C&A notes, it merely stated that the construction of the claims did not matter for purposes of its IPR." (citation omitted)).

[15] *See, e.g.*, **Ex. F**: Excerpts from Petition for IPR of '633 Patent (IPR2022-00252) at 80 (identifying "Ryu's disclosure of a JFET width 'from about 1 [micrometer] to about 10 micrometers],'" which clearly falls within any possible construction of "about 3").

before this Court is whether the upper and lower boundaries of the claim are sufficiently clear.

E. The Court should disregard Purdue's "request" to exclude Dr. Subramanian.

At the end of its responsive brief, Purdue argues that Dr. Subramanian should be excluded under *Daubert*. Since Purdue failed to file a proper *Daubert* motion on this issue, the Court should disregard this request. To the extent that Purdue implies the Court should discount ST's expert's testimony, Purdue is incorrect. Dr. Subramanian has the requisite knowledge and experience. First, even general knowledge and experience in semiconductor and wide bandgap devices suffices here. *See Hologic, Inc. v. Minerva Surgical, Inc.*, 764 F. App'x 873, 879 (Fed. Cir. 2019) (holding that, although the claims were directed to uterine ablation, "a skilled artisan was someone who had 'experience developing or implementing electrosurgical devices' generally rather than uterine devices specifically"). The specifications and prosecution histories of the patents teach that the issues relevant to the disputed terms are not uniquely and specifically directed to silicon-carbide devices, one of many types of semiconductor devices. (Subramanian Rebuttal Decl. ¶¶ 5–8.) As such, a POSITA's experience should be directed to semiconductor devices generally, not just semiconductor devices that include silicon-carbide. In addition, silicon carbide MOSFETS are just one type of wide bandgap device. Purdue incorrectly states that "none of the publications and patents listed on [Dr. Subramanian's] CV relate to wide bandgap devices." Dr. Subramanian's CV shows that he has researched and published numerous papers on wide bandgap devices for more than a decade. By any measure, regardless of the precise definition of a POSITA, Dr. Subramanian is more than qualified as a POSITA. The Court should disregard Purdue's request to exclude his opinions.

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Respectfully submitted:

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CERTIFICATE OF SERVICE

I certify that on March 28, 2022, the foregoing document was served via electronic mail on counsel of record for Plaintiff.

/s/ Justin S. Cohen
Justin S. Cohen